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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/037,844

10/19/2001

Kuang-Chien Chen

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11/19/2002

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SAN JOSE, CA 95110

EXAMINER

LEVIN, NAUM B

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/037,844

Applicant(s)

CHEN ET AL.

Examiner

Naum B Levin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 12-22 and 29-34 is/are rejected.
- 7) ☒ Claim(s) 6-11 and 23-28 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \*   c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.                      6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claim 31 is objected to because of the following informalities:

in line 1 claim should be referenced to claim --18-- instead to claim 26.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-5, 14-22 and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Lockyear (US Patent 6,336,206).

Lockyear discloses method and apparatuses for structural input/output matching for design verification including:

(1), (18) A method, a computer-readable storage medium having stored thereon computer instructions for modeling a circuit designs comprising:

synthesizing a circuit design to create a first gate-level representation of the circuit design (col.1, ll.33-37);

analyzing a second gate-level representation of the circuit design to learn architecture information (col.1, ll.37-39 and ll.48-60); and

resynthesizing the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design (col.1, ll.39-41);

(2), (19) The method, a computer-readable storage medium having stored thereon computer instructions, wherein the second gate-level representation being created during a synthesis process (col.1, ll.36-38 and ll.44-50);

(3), (20) The method, a computer-readable storage medium having stored thereon computer instructions, wherein the learned architecture information comprises logic network architecture in the second gate-level representation of the circuit design (col.2, ll.37-60);

(4), (21) The method, a computer-readable storage medium having stored thereon computer instructions, wherein the analyzing comprises a resource sharing learning (col.3, ll.59-67);

(5), (22) The method, a computer-readable storage medium having stored thereon computer instructions, wherein the resource sharing learning comprising:

creating one or more resource pairs from sharable resources in the first gate-level representation of the circuit design (col.7, ll.52-55);

for each of the one or more resource pairs, synthesizing a subcircuit that shares the resource pair (col.5, ll.55-57 and col.13, ll.9-13);

for each of the synthesized subcircuits, calculating a similarity with a corresponding subcircuit in the second gate-level representation of the circuit design (col.1, ll.44-50 and col.12, ll.26-34);

identifying the synthesized subcircuits having a high similarity with the corresponding subcircuit in the second gate-level representation of the circuit design (col.13, ll.21-46); and

resynthesizing the first gate-level representation of the circuit design to include the subcircuits identified as having high similarity (col.1, ll.39-41 and col.13, ll.48-52);

(14), (31) The method, a computer-readable storage medium having stored thereon computer instructions, wherein the analyzing comprising:

identifying a first subcircuit in the first ate-level representation of the circuit design (col.5, ll.55-57 and col.13, ll.9-13);

identifying a second subcircuit in the second gate-level representation of the circuit design, the second subcircuit corresponding to the first subcircuit (col.1, ll.44-50 and col.12, ll.26-34); and

calculating a similarity between the first subcircuit and the second subcircuit (col.1, ll.44-50 and col.12, ll.26-34);

(15), (32) The method, a computer-readable storage medium having stored thereon computer instructions, wherein calculating the similarity comprises checking one or more circuit structures (col.7, ll.26-32);

(16), (33) The method, a computer-readable storage medium having stored thereon computer instructions, wherein calculating the similarity comprises checking one or more boolean functions (col.2, ll.13-21);

(17), (34) The method, a computer-readable storage medium having stored thereon computer instructions, wherein calculating the similarity comprises performing one or more simulations (col.1, ll.29-31).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12, 13, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lockyear in view of Sharma et al. (US Patent 5,841,663).

5. With respect to claims 12, 13, 29 and 30 Lockyear teaches the features above but lacks a method and a computer-readable storage medium having stored computer instructions, wherein analyzing comprises an merging operator.

Sharma discloses apparatus and method for synthesizing integrated circuits using parameterized HDL modules including:

(12), (29) The method, a computer-readable storage medium having stored computer instructions, wherein the analyzing comprises an operator merging learning (col.18, ll.8-9);

(13), (30) The method, a computer-readable storage medium having stored computer instructions, wherein the operator merging learning comprising:

expressing a complex operation in the first gate-level representation as a summation (col.16, ll.7-25);

analyzing a reduction tree structure in the second gate-level representation of the circuit design, the reduction tree corresponds to the complex operation (col.13, ll.58-67 and col.14, ll.28-37); and

resynthesizing a reduction tree in the first gate-level representation from the reduction tree structure learned from the second gate-level representation (col.18, ll.8-20; col.27, ll.30-39 and col.28, ll.22-39).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Sharma's teaching regarding the method and a computer-readable storage medium having stored computer instructions, wherein analyzing comprises an merging operator and use it in Lockyear's invention to improve efficiency and speed of the integrated circuit design.

***Allowable Subject Matter***

6. Claims 6-11, and 23-28 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


**Conclusion**

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L  
November 6, 2002

  
SMITH  
EXAMINER  
10300